|  |  |
| --- | --- |
| Danfysik 2016 | |
| Addendum to Detailed Design Report | |
|  |  |
|  |  |
| Raster scanning magnet system for ESS | |

**Addendum to DDR RSMS**

Rev A

DF project no: 502446

|  |  |  |
| --- | --- | --- |
| Preparation/Review | Signature | Date |
| Author: |  |  |
| Alexander Elkiær | PAEL | 2017-02-20 |

Revision History Log:

|  |  |  |  |
| --- | --- | --- | --- |
| Date: | Rev.: | Init: | Changes: |
| 2017-02-20 | A |  | Initial version |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

Reference Documents

* 502446\_CDR\_RevA\_Review\_Report\_Response\_hdt.xls point ID 30

Content

Page

[1. Introduction 3](#_Toc475369415)

[2. Second Response to ID-30 data 4](#_Toc475369416)

[2.1. Current generation 4](#_Toc475369417)

[2.2. Hand checking signals 4](#_Toc475369418)

[2.3. Current LOOP constrains 5](#_Toc475369419)

[2.4. Capacitor storage 5](#_Toc475369420)

[2.5. Changing current on the fly to a lower value 5](#_Toc475369421)

[2.6. Changing current on the fly to a higher value 5](#_Toc475369422)

[2.7. Changing pulse frequency on the fly to a lower value 6](#_Toc475369423)

[2.8. Changing pulse frequency on the fly to a Higher value 6](#_Toc475369424)

[3. Second Response to ID-30 Conclusion 6](#_Toc475369425)

# Introduction

Point ID30 from the file “502446\_CDR\_RevA\_Review\_Report\_Response\_hdt.xls” requires a more detail description, which is given in this document.

|  |
| --- |
| Request from ESS |
| A RSM parameter tuning scenario is not the typical operation of the supply, but it should nevertheless be anticipated. It is thus preferable that if the system state is not correct, the supplies should still raster but merely give a hardware warning signal. Supplies should always try to deliver a pulse. Supply operation should only halt and require a reset in case of potential self-damage! |

|  |
| --- |
| Danfysik’s response |
| Small changes of output current and raster frequency can be made on-the-fly without interrupting the operation of the power supply.  Large changes will require large changes in voltage and time to settle (in which the power supply should not operate). Especially changing frequency from a high frequency to a lower frequency requires a pause in rastering, since low frequency rastering at full voltage would result in dramatic over-current.  Therefore, rastering will be inhibited if voltage is more than 2% different from the required voltage (after changing the set current and/or frequency). In other words, fast changes in set current or set frequency larger than 2% may cause the power supply to inhibit rastering until voltage settles to the new value.  Furthermore, if the DC-Link voltage is lower than +2% from desired value, pulsing is enabled by setting the "Trig Permit" signal but the "Beam Permit" will only be given when 1% accuracy can be guaranteed. (The only way to remove the rest of the DC-Link capacitor energy.) After a burst, the I-READY signal will tell, if the burst was within the 1% specification. |

|  |
| --- |
| Follow up question from Heine |
| If ESS insists on it, could this behavior not easily be changed to match the customer request: Supply operation should always try to deliver a burst and require a reset in case of potential self-damage? What would be the problem with broadening the 2% operational window, apart from delivering bursts with wrong amplitude? Leave it to ESS to decide whether to send the beam |

|  |
| --- |
| Danfysik second response |
| Below is Danfysik’s second response where different scenarios are described along with the raster power supply working principles |

# Second Response to ID-30 data

## Current generation

Applying a voltage to an inductor, the current through it increase according to the formula:

Given that the resistive value of the coil is negligible.

As the voltage can be seen as constant throughout the burst period, the formula can be written as:

## Hand shaking signals

Bursts are controlled through some hand shaking signals realized through light guide signals.

Quickly explained they work as follows (given that the power supply is turned ON and everything is OK):

Hand shaking signals:

|  |  |  |
| --- | --- | --- |
| Signal | I/O | Purpose |
| Pre-Trig | I | Make a burst when trigged |
| Trig Permit | O | Everything OK for a burst: - VRDY <±H% - Power is ON  - Supply is Enabled  - Minimum time since prev. burst has elapsed |
| Beam run permit | O | Set active if: - VRDY <±L% - IRDY Active - X number of pulses has elapsed |
| Polarity Input | I | Start at given polarity - High=“positive”  - 10kHz=”negative” (no light will result in “negative" pulses, and an error flag) |
| I-Ready | O | Output current for last burst was within 1% of set value |
| Enable Operation | I | Must be active to enable bursts. - If inactive, disable H-Bridge and operation |

Where H% is 2-4% and L% is 0.2%. Both values will be optimized during tests

A new set value (frequency or current) will charge or dis-charge the capacitor bank to predicted voltage level. During this time until the voltage accuracy is within 4%, no “Trig Permit” is given.

When the capacitor voltage level reaches within 4% accuracy the “Trig Permit” signal is given and pulsing is allowed. The “Beam Run Permit” will not be given until the capacitor voltage reaches below L% and the accuracy thereby granting the output accuracy level. Pulsing from +H% to +L% is the only way to discharge the capacitor bank.

## Current LOOP constraints

The current level of the pulses burst-to-burst is regulated by a digital loop within the FPGA. Due to the nature of 14Hz pulsing and the Nyquist stability criteria, the loop response is made accordingly slow (sampling rate of 14Hz). Taking this fact into consideration, entering the required stability level may take some time and when driven far away from the set value, it may lead to excessive overshoots.

## Capacitor storage

The energy to perform a burst is taken from a capacitor bank. To ensure accurate pulses throughout the burst, the capacitor bank is made quite powerful.

As the input converter can only charge the capacitor bank, an independent bleeder circuit is added enabling discharging (if the voltage is above H% of the desired set value).

To ensure that charging and bleeding is not active at the same time, a given window margin is implemented, which is ensured by the H%. This value is at present 4% as best choice and will be optimized during tests.

## Changing current on the fly to a lower value

Changing the current from 100% to 50%, the capacitor storage bank voltage must be reduced to half of the previous value. The capacitor bank voltage set value is reduced by the FPGA and the capacitor charge supply will stop charging and the bleeder circuit will start.

If bursts are allowed during the discharge process, pulses up to twice the desired value in this example will be generated.

## Changing current on the fly to a higher value

Changing the current from 50% to 100%, the capacitor storage bank voltage must be increased to twice of the previous value. The capacitor bank voltage set value is doubled by the FPGA and the capacitor charge supply will start charging.

If bursts are allowed during the charge process pulses much lower amplitude of the desired value will be generated.

As energy is being used for pulsing and not only for charging the overall charging process will be extended, and thereby the time until the power supply will be operational at the desired level, be increased many folds.

If bursting during the charging process, the loop will calculate (with good reason) that the output voltage is too low, and thereby increase the given predicted voltage set value. Due to the slow and increased charge time, this will lead to a significant overshoot, that may trip the power supply with an over current interlock.

## Changing pulse frequency on the fly to a Lower value

Changing the frequency to a lower value is the same as increasing ∆t in the formula given in chapter 2.1. So changing the frequency from 40KHz to 20kHz will double the ON time resulting in a 100% current over shoot (3\*340A if running at 100%) thereby interlocking the power supply.

## Changing pulse frequency on the fly to a Higher value

Changing the pulse frequency from 20kHz to 40kHz, the capacitor storage bank voltage must be increased to twice of the previous value. The scenario is therefore the same as for chapter 2.5 “Changing current on the fly to a higher value”.

# Second Response to ID-30 Conclusion

It is not easy to change defined working behavior. The power supply must protect itself and ensure that misuse is not allowed.

Broadening the 2% “±H%”-margin is possible, and final tests will show how much.

Attention should the payed to the “Beam Permit” signal. If not telling that a good burst can be produced what else should this signal be good for?

Whether or not an issued burst was within the specification level can be read from the I-READY signal.